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REMARKS

The following discussion addresses the objections and rejections set out in the Office Action under reply in the same order as presented in that office action.

In Section 2 of the Office Action, claim 2 was objected to because the period at the end of the claim was missing. By this amendment, the missing period is added to claim 2.

In Section 4 of the Office Action, claims 1-4, 8-10 and 17-21 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting in view of claims found in copending Applications 10/673,712 and 10/673,713. As the Examiner correctly found, the prosecution of these copending applications is ongoing. Consequently, the claims of these copending applications may change; and it is premature to reject claims of the instant application on the ground of double patenting until prosecution of those applications has been completed. Moreover, it is noted the Examiner has not attempted to explain why, in his view, the claims of the instant application are obvious in view of the claims of the copending applications. On the contrary, and as an example, it is seen that claim 1 of the instant application differs from claim 1 of the '712 application and also differs from claim 1 of the '713 application in a non-obvious manner. Claim 1 of the '713 application recites the storage and use of a software phase-locked loop program, which is not recited in claim 1 of the instant application. Claim 1 of the '712 application recites synchronizing data segments to align them to a frame or predetermined pattern to determine a bit error rate, and comparing each of the data segments to the predetermined pattern on a bit by bit basis, which is not found in claim 1 of the instant application. It is submitted, therefore, that the claims of the present application are not obvious in view of the claims of these copending '712 and '713 applications; and the premature provisional double patenting rejection should be withdrawn.

PAGE 9/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20

In Section 6 of the Office Action, claims 1-21, all the claims remaining for consideration, were rejected under 35 USC 103 as being obvious in view of published U.S. application 2001/0021151 (Verboom). It is respectfully submitted that one of ordinary skill in the art, after reading and understanding Verboom, would not be enabled by that reference to make and use the invention defined by Applicants' claims 1-21.

Turning to claims 17-20, these claims are directed to an apparatus for **displaying** an eye diagram. While Verboom mentions an "eye-pattern" at paragraph [0007], he clearly provides no teaching of apparatus for displaying an eye diagram in response to an acquired data signal. Thus, at the outset, Verboom provides no teaching, suggestion or hint of Applicants' claimed invention and clearly does not render claim 17 obvious.

In addition, Verboom fails to suggest the acquisition unit of claim 17, which operates to "acquir[e] a data signal for a predetermined time." In Verboom, the data signal that is "acquired" is read from a storage device, it is either a digitized signal 202 or a digitized read analog signal (see, for example, paragraph [0070] and paragraph [0084]). There is, however, no suggestion in Verboom, and particularly at the locations identified by the Examiner (abstract and paragraph [0091]), of acquiring a data signal "for a predetermined time."

Verboom also fails to suggest "a memory of said test instrument for storing said data signal," as recited in claim 17. The Examiner refers to paragraphs [0133] and [0084] of Verboom as teaching such a memory. It appears the Examiner is relying upon registers 602, 604, shown in Fig. 6A of Verboom as constituting a memory in which the acquired data signal is stored. However, Verboom describes these registers as simply imparting a 1-bit delay to the digitized signal for the purpose of permitting channel bits that are a predetermined distance from

PAGE 10/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20

one another to be compared (see the penultimate sentence in paragraph [0091]). Clearly, a 1-bit delay circuit is not a "memory," as claimed.

Still further, Verboom does not teach "a clock recovery unit for recovering a clock signal from said stored data signal," as recited in Applicants' claim 17. Paragraph [0069] of Verboom describes Fig. 2, which shows a channel clock 204. This channel clock is not recovered from the stored, acquired signal, as is specified in Applicants' claim 17. Indeed, if the Examiner's argument is followed, Verboom's clock must be recovered from the 1-bit delayed signal that appears at the output of register 602 or 604. This clearly is not the case; and it must be emphasized that Verboom does not recover a clock signal from the stored, acquired data signal.

Nor does Verboom suggest "a processor for slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal." In applying Verboom to this limitation recited by Applicants' claim 17, the Examiner relies upon slicer 410, shown in Verboom's Fig. 4 and described at paragraphs [0091] - [0094]. But, slicer 410 is a classical slicer to determine whether a waveform is a "1" or a "0" depending upon whether the waveform is above or below a slicing level. Slicer 410 does not slice the delayed input signal from 1-bit delay 404 into segments of predetermined length. This is evident from Figs. 5A-5P, which show 2T marks and spaces, 3T marks and spaces, and long marks and spaces (see, in particular, paragraphs [0094] - [0131]). Consequently, the marks and spaces produced by slicer 410 are not "data segments of a predetermined length."

Finally, and as mentioned above, Verboom does not teach "a display for overlaying said plurality of data segments in a time synchronized manner," as recited in claim 17. This results in the display of the eye diagram; and Verboom is not concerned with displaying an eye diagram derived from an acquired data signal. The Examiner recognizes this deficiency of Verboom,

PAGE 11/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20

("Verboom does not disclose displaying the plurality of data segments," *see page 5 of the Office Action*), yet concludes, in the absence of any prior art teaching or factual support, that it would be obvious "to display the data to allow a user to make adjustment." Why would it be obvious? Where is the motivation in Verboom to display the eye diagram from the acquired data signal? Why would Verboom, who compensates for the effect of inter-symbol interference, even want to display the eye diagram, which does not, by itself, provide any compensation?

It is respectfully submitted the Examiner merely has concluded it would be obvious to do what Applicants do because he has found no suggestion in the prior art to do so. This naked assertion of obviousness is the very hindsight reconstruction of Verboom that has consistently been prohibited by the USPTO Board of Patent Appeals and Interferences and by the Court of Appeals for the Federal Circuit.

Therefore, since Verboom fails to describe or suggest all of the limitations recited by Applicants' claim 17, it is respectfully submitted that Verboom does not render claim 17 obvious. Consequently, the withdrawal of the rejection of claim 17 is respectfully requested.

Claims 18-20 all depend, either directly or indirectly from claim 17. Accordingly, these dependent claims include all of the limitations recited by claim 17; and for at least this reason alone, these dependent claims are patentably distinct over Verboom. It is noted, the Examiner has not offered a separate rejection or reason for his denial of claims 18-20.

Claim 21 is a dependent claim that depends from claim 17. The Examiner offers additional reasoning in support of his rejection of claim 21. However, upon reviewing those portions of Verboom particularly cited by the Examiner to support his rejection of claim 21, it is submitted that Verboom fails to disclose (at those portions) the features ascribed by the Examiner to Verboom. For example, claim 21 states that the clock recovery unit "determines

PAGE 12/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20

pairs of adjacent samples that straddle said vertical threshold." The Examiner relies upon paragraph [0105] of Verboom to allegedly describe this feature. This paragraph refers to a Cond0 and a Cond1 separated by an undefined sample, and the evaluation of in-between and other adjacent samples. It is not understood how this discloses the feature of determining pairs of adjacent samples that straddle the vertical threshold.

In addition, claim 21 states that the clock recovery unit "estimates a time of crossing said vertical threshold between said adjacent samples to obtain a series of observed times of threshold crossing." The Examiner asserts that paragraph [0131] of Verboom describes this estimation feature. But paragraph [0131] makes no mention of any estimation whatsoever. There is no teaching, implication, inference or suggestion in paragraph [0131] of **estimating** a time of crossing of a vertical threshold between adjacent samples.

Therefore, since Verboom is silent with respect to recitations of claim 21, and since there is no prior art suggestion that would motivate one to modify Verboom to incorporate the features of these recitations, it is submitted that claim 21 is patentably distinct over Verboom and the rejection of claim 21 as being obvious in view of Verboom should be withdrawn.

Claim 1 is an independent claim directed to apparatus that is similar to the apparatus recited by claim 17, except claim 1 does not recite the display that is recited in claim 17. The Examiner rejected claim 1 as being obvious in view of Verboom, "under similar rationale as set forth in claim 17" (see the bottom of page 5 of the Office Action). Therefore, inasmuch as the Examiner has not provided a separate basis for rejecting claim 1, it follows that claim 1 is patentably distinct over Verboom for many of the same reasons that have been presented in the foregoing discussion of claim 17, namely, Verboom's failure to suggest the "acquisition unit," the "memory," the "clock recovery unit" or the "processor for slicing said stored data signal into

PAGE 13/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20

a plurality of data segments of a predetermined length in accordance with said recovered clock signal" recited in both claim 17 and claim 1.

Claims 2-4 were rejected "under similar rationale as set forth in claim 21." Consequently, claims 2-4 are patentably distinct over Verboom for the same reasons discussed above in connection with claim 21.

Claims 5-9 were rejected as being obvious in view of Verboom. However, the Examiner's explanation of his rejection of these claims is limited to claim 9. The asserted portions of Verboom, relied upon by the Examiner in his rejection of claims 5-9, fail to suggest the recitations of claim 5, namely, "wherein said clock recovery unit further considers a hysteresis requirement to confirm ...". It is not seen where, in Verboom, there is a teaching of any hysteresis requirement that is used by a clock recovery unit. Therefore, claim 5 is unobvious over Verboom because the reference fails to disclose the aforequoted feature of claim 5; and there is no prior art suggestion to reconstruct Verboom to incorporate this feature.

Claims 6-8 depend from claim 2. That claim 2 is unobvious over Verboom has been discussed above. It follows, then, that claims 6-8 likewise are unobvious over this reference; and the rejection of claims 6-8 should be withdrawn.

In rejecting claims 5-9, the Examiner alleges that Verboom discloses elements that are found in Applicants' claim 9. Paragraphs [0006]-[0013] of Verboom are relied upon by the Examiner as allegedly teaching a clock recovery unit that compares the series of observed times of threshold crossing "to an ideal perfectly periodic sequence of expected times of threshold crossing ..." and that "determines an error between said observed times and said expected times." It is not seen where or how these paragraphs of Verboom teach or even suggest the aforequoted functions of Applicants' claimed clock recovery unit. Still further, the Examiner

relies on paragraphs [0012] - [0090] of Verboom as an alleged teaching of a clock recovery unit that "adjusts the phase of said recovered virtual periodic clock in accordance with said determined error." It is not seen where, in these paragraphs, there is a suggestion of adjusting the phase of a recovered virtual clock in accordance with the error between observed and expected times of threshold crossings, as recited in claim 9. Consequently, Verboom does not enable one of ordinary skill in the art to make and use the apparatus of claim 9; and claim 9 is unobvious over Verboom. The withdrawal of the rejection of claim 9 is respectfully solicited.

Claims 10-16 were rejected on the ground that Verboom's paragraphs [0012] - [0090] describe the features recited by these claims. Claims 10, 14, 15 and 16 are directed to features of the clock recovery unit. As mentioned above, Verboom does not describe a clock recovery unit. Furthermore, it is submitted that paragraphs [0012] - [0090] do not describe the clock recovery unit features recited in claims 10, 14, 15 and 16. Therefore, Verboom is not evidence of the obviousness of these claims.

Claims 11, 12 and 13 are directed to features of the processor and its operation in connection with determining expected transition times. The Examiner correctly did not explain how Verboom is suggestive of the features recited in these claims -- Verboom simply does not describe these features in a manner that would enable one of ordinary skill in the art to make and use the inventions defined by claims 11, 12 and 13. Therefore, since these claims are unobvious over Verboom, the withdrawal of the rejection thereof is respectfully solicited.

Statements appearing above in respect to the disclosures in the cited references represent the present opinions of the undersigned attorney and, in the event the Examiner disagrees with any of such opinions, it is respectfully requested that the Examiner specifically indicate those portions of the references providing the basis for a contrary view.

PAGE 15/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20

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PAGE 16/16 * RCVD AT 10/10/2006 3:48:40 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/44 * DNIS:2738300 * CSID:2125880500 * DURATION (mm-ss):06-20